CLAIMS

1. A cross-talk cancellation method using a main signal (62) associated with a target track (32) and satellite signals (61, 63) associated with side tracks (31, 33), said main signal showing transitions (X_m) and runs of various lengths ($d_{m+1,m}$) between two transitions (X_m, X_{m+1}), said cancellation method comprising the steps of:

- filtering said satellite signals with adaptive filters (71, 73), thereby generating filtered versions (81, 83) of said satellite signals,
- updating the coefficients of said adaptive filters by minimizing the mismatch between the actual and the expected run length between two transitions of the main signal, and
- processing said main signal, thereby generating an improved main signal (102), said processing including a subtraction of said filtered versions of said satellite signals.

2. A program comprising instructions for implementing a cross-talk cancellation method as claimed in claim 1 when said program is executed by a processor.

3. A signal processor (40) comprising cross-talk cancellation means (42) for receiving a main signal (62) associated with a target track (32) and satellite signals (61, 63) associated with side tracks (31, 33), said main signal showing transitions (X_m) and runs of various lengths ($d_{m+1,m}$) between two transitions (X_m, X_{m+1}), said cross-talk cancellation means comprising:

- filtering means (71, 73) for filtering said satellite signals with adaptive filters, thereby generating filtered versions (81, 83) of said satellite signals,
- updating means (111, 113) for updating the coefficients of said adaptive filters by minimizing the mismatch between the actual ($d_{m+1,m}$) and the expected ($d^{(exp)}_{m+1,m}$) run length between two transitions of the main signal, and
- processing means (93) for generating an improved main signal (102) from said main signal by subtraction of said filtered versions of the satellite signals.

4. A signal processor as claimed in claim 3, comprising a fixed clock (55), time recovery means (130), and a bit clock (120) driven by said time recovery means, said fixed clock being asynchronous with respect to said bit clock, wherein said cross-talk cancellation means are operated at said fixed clock.

5. A signal processor as claimed in claim 4, wherein said bit clock has a bit clock frequency and said fixed clock has a fixed clock frequency that is substantially different from said bit clock frequency such that the ratio between said bit clock frequency and said fixed clock frequency is substantially different from 1, said signal processor further comprising time recovery means (50-1, 50-2) for estimating said ratio and providing said ratio to said updating means, said updating means being designed to take said ratio into account for updating said coefficients.

6. An apparatus (6-1, 6-2) for reading a signal stored along a track on a storage medium (1) comprising a signal processor as claimed in claim 3.

7. An apparatus for reading a signal stored along a track on a storage medium comprising a signal processor as claimed in claim 4.

8. An apparatus for reading a signal stored along a track on a storage medium comprising a signal processor as claimed in claim 5.